instructions configured to supply the test vector data to good samples and faulty samples;

instructions configured to determine a range of pass/fail decision criteria and effective address pairs for testing semiconductor devices in a manufacturing process;

instructions to apply test vectors of the effective address pairs to a semiconductor device; and

instructions to specify a faulty part within the semiconductor device by measuring an emission from the semiconductor device.

REMARKS

By the present Amendment, Applicant amends claims 1-19 to more appropriately define the present invention. In accordance with the requirements of 37 C.F.R. § 1.121(c)(1), Applicant provides a marked-up version of the amended claims in an attached Appendix. No new matter has been added by these amendments. Claims 1–19 remain pending.

In the Final Office Action, the Examiner rejected claims 1-19 under 35 U.S.C. §103(a) as unpatentable over U.S. Patent No. 5,694,063 to Burlison et al. (*Burlison*) in view of U.S. Patent No. 4,635,259 to Schinabeck et al. (*Schinabeck*).

Applicant respectfully disagrees with the Examiner's arguments and conclusions and respectfully traverses the 35 U.S.C. §103(a) rejection for the following reasons.

A *prima facie* case of obviousness has not been made, since the Examiner does not show that all the elements of Applicant's claims are met in the cited references. The

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Examiner also does not show that there is any suggestion or motivation to modify the cited references to result in the claimed invention nor a reasonable expectation of success in doing so. "To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art." *See* M.P.E.P. §2143 (8th Ed. 2001). The Examiner does not show that all the elements of Applicant's claims are met in the cited references, taken alone or in combination, and does not show that there is any suggestion or motivation to modify the cited references to result in the claimed invention, or any reasonable expectation of success from so doing.

Burlison describes a method and apparatus for determining the quiescent power supply current of a "device under test". (*See* Abstract). By detecting "the slope of the time rate of change in voltage for a node" and comparing voltages measured before and after decoupling a power supply from the node, *Burlison* increases the speed of I_{DDQ} testing. (*See* col. 3, ll. 65-67 and col. 4, ll. 1-5). In other words, *Burlison* teaches determining the time rate of change for voltage in one device. In addition, *Burlison* uses an automatic test equipment (ATE) for generating test patterns or test vectors inputted to a device under the test. (*See* col. 7, ll. 5-8; col. 8, ll. 5-6; FIG. 7; and FIG. 8).

Schinabeck describes "a method and apparatus for applying analog voltages or currents to nodes of a device under test." (*See* col. 3, ll. 22-25). Further, *Schinabeck* describes monitoring resulting currents or voltages with the purpose of evaluating electrical characteristics of the device under the test. According to *Schinabeck*, the

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described method and apparatus increase test rates by reducing the impact of analog setting time. (*See* Col. 3, ll. 22-29).

Independent claim 1 is directed to a semiconductor testing apparatus for testing semiconductor devices comprising, *inter alia*, "a read circuit configured to read measurement data including a test vector data and data of good samples and data of faulty samples returned to a manufacturer."

Indeed, neither *Burlison* nor *Schinabeck* teaches or suggests at least a read circuit configured to read measurement data including data of good samples and data of faulty samples returned to a manufacturer. *Burlison*, for example, does not even mention faulty samples returned to a manufacturer. Nor does *Schinabeck* disclose such a feature. Furthermore, combining those references will not treat this deficiency. Therefore, the obviousness rejection is improper and must be withdrawn. Thus, Applicant submits, the Examiner's reliance on *Burlison* and *Schinabeck* fails to establish *prima facie* obviousness under 35 U.S.C. § 103(a) of claim 1.

Claims 2-4 depend from allowable claim 1 and include all the elements thereof and are allowable at least by virtue of their dependence from allowable claim 1.

Claim 5 is directed to a semiconductor testing method for testing semiconductor devices comprising, *inter alia*, "reading measurement data including a test vector data and data of good samples and faulty samples returned to a manufacturer" and "supplying the test vectors to the good samples and the faulty samples." Both *Burlison* and *Schinabeck* fail to teach or suggest at least reading measurement data of good

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samples and faulty samples returned to a manufacturer as discussed above with respect to claim 1. Therefore, the Examiner's reliance on *Burlison* and *Schinabeck* fails to establish *prima facie* obviousness under 35 U.S.C. § 103(a) of claim 5.

Claims 6 - 8 depend from allowable claim 5 and include all the elements thereof and are allowable at least by virtue of their dependence from allowable claim 5.

Claim 9 is directed to a program with which a semiconductor testing method for testing semiconductor devices is executed by a computer in a semiconductor testing apparatus comprising, *inter alia*, "instructions configured to read measurement data including a test vector data and data of good samples and faulty samples returned to a manufacturer." Again, neither *Burlison* nor *Schinabeck* teaches or suggests at least instructions configured to read measurement data of good samples and faulty samples returned to a manufacturer as discussed above with respect to claim 1. And therefore, again, the Examiner's reliance on *Burlison* and *Schinabeck* fails to establish *prima facie* obviousness under 35 U.S.C. § 103(a) of claim 9.

Claims 10-12 depend from allowable claim 9 and include all the elements thereof and are allowable at least by virtue of their dependence from allowable claim 9.

Claim 13 is directed to a semiconductor testing method of specifying a faulty part in a semiconductor device comprising, *inter alia*, "reading measurement data wherein the measurement data includes a test program, test vector data, data of good samples and faulty samples returned to a manufacturer." Once again, both *Burlison* and *Schinabeck* fail to teach or suggest at least reading measurement data wherein the

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measurement data includes data of good samples and faulty samples returned to a manufacturer as discussed above with respect to claim 1. Thus, the 35 U.S.C. § 103(a) rejection of claim 13 is improper and must be withdrawn.

Claims 14 and 15 depend from allowable claim 13 and include all the elements thereof and are allowable at least based on such dependency.

Claim 16 is directed to a semiconductor testing apparatus for specifying a faulty part in a semiconductor device comprising, *inter alia*, "a read circuit configured to read measurement data wherein the measurement data includes a test program, test vector data, data of good samples and faulty samples returned to a manufacturer." Neither *Burlison* nor *Schinabeck* teaches or suggests at least a read circuit configured to read measurement data wherein the measurement data includes data of good samples and faulty samples returned to a manufacturer. Thus, the Examiner's reliance on *Burlison* and *Schinabeck* fails to establish *prima facie* obviousness under 35 U.S.C. § 103(a) of claim 16.

Claims 17 and 18 depend from allowable claim 16 and include all the elements thereof and are allowable at least by virtue of their dependence from allowable claim 16.

Finally, claim 19 is directed to a program with which a semiconductor testing method is executed by a computer in a semiconductor testing apparatus which comprises a read circuit, a determination circuit, and a faulty part specifying circuit, the program comprising, *inter alia*, "instructions configured to read measurement data wherein the measurement data includes a test program, test vector data, data of good

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samples and faulty samples returned to a manufacturer." As discussed above with respect to claim 1, both *Burlison* and *Schinabeck* fail to teach or suggest at least instructions configured to read measurement data wherein the measurement data includes data of good samples and faulty samples returned to a manufacturer. Therefore, the Thus, the 35 U.S.C. § 103(a) rejection of claim 19 is improper and must be withdrawn.

In view of the foregoing, Applicant respectfully submits that the 35 U.S.C. § 103(a) rejections of claims 1–19 are improper and should be withdrawn. Applicant respectfully submits that pending claims 1–19 are in condition for allowance.

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If there are any fees due under 37 C.F.R. § 114, which are not enclosed, including any fees required for an extension of time under 37 C.F.R. § 1.136, please charge such fees to our deposit account 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER, L.L.P.

Dated: January 6, 2003

By: Richard V. Burgujian, Reg No 24,014
for Richard V. Burgujian
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APPENDIX TO AMENDMENT OF JANUARY 6, 2003
VERSION WITH MARKINGS TO SHOW CHANGES MADE

AMENDMENTS TO THE CLAIMS

Please amend claims 1 through 19 as follows:

1. (Amended) A semiconductor testing apparatus for testing semiconductor devices comprising:

a read circuit [for] configured to read[ing] measurement data including a [plurality of] test vector[s] data and data of good samples and data of faulty samples returned to a manufacturer;

[a measurement circuit for supplying the test vectors to semiconductor devices and for measuring a current value output from the semiconductor devices corresponding to each address of each test vector;

a calculation circuit for calculating a current-value change rate per address pair consisting of different two addresses;]

a determination circuit [for] configured to supply the test vector data to the good samples and the faulty samples, and to determine [determining] a range of pass/fail decision criteria and effective address pairs for testing [to be used for deciding whether a] semiconductor devices [as a target test device to be tested is a good sample or a faulty sample based on current-value change rates obtained by supplying the plurality of test vectors to good samples as semiconductor devices]; and

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[a decision circuit for comparing current-value change rates obtained by supplying the plurality of test vectors to faulty samples with the range of pass/fail decision criteria per address pair, and for deciding whether the target test device is a good sample as a non-defective semiconductor device or a faulty sample based on the current-value change rates corresponding to the address pairs extracted based on the comparison results obtained.]

an IDDQ measuring circuit configured to test semiconductor devices by applying the effective test vector.

2. (Amended) [A semiconductor testing device according to] The apparatus of claim 1 wherein the determination circuit comprises: [determines the range of pass/fail decision criteria based on the current-value change rates obtained from the plurality of good samples.]

a changing rate calculation circuit configured to select address pairs from the test vector data, to supply the address pairs to the good samples and the faulty samples, to measure current-values of the good samples and faulty samples, and to calculate changing rates of each of the good samples and faulty samples;

a range criteria determination circuit configured to determine a range of pass/fail decision criteria by using the changing rates of each of the good samples;

a comparing circuit configured to compare the changing rates of each of the faulty samples to the range of pass/fail decision criteria, and to determine whether the

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changing rates of each of the faulty samples fall outside of the range of the pass/fail decision criteria; and

an effective address pair determination circuit configured to determine the changing rate falling outside of the range of pass/fail decision criteria, and to select an address pair which makes the faulty samples provide the changing rate falling outside of the range of pass/fail decision criteria as an effective address pair.

3. (Amended) [A semiconductor testing device according to] The apparatus of claim 1, wherein the IDDQ measuring circuit comprises:

[the determination circuit comprising a measurement range determination circuit for comparing current-value change rates of the faulty samples obtained by supplying the plurality of test vectors to the faulty samples with range of pass/fail decision criteria per address pair, and for extracting the address pairs corresponding to the current-value change rates of the faulty samples that are outside of the range of pass/fail decision criteria from the plurality of address pairs in the plurality of test vectors, and for determining effective address pairs as an address pair group to be effectively used for the pass/fail decision,

wherein

the measurement circuit supplies the test vectors corresponding to the address pair group to the target test device.]

a tester configured to: acquire the effective address pair, supply test vectors corresponding to the effective address pair to the semiconductor device, measure

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current-value output of the semiconductor device, and calculate changing rates of the semiconductor device; and

a decision circuit configured to determine a changing rate falling outside of the range of pass/fail decision criteria.

4. (Amended) [A semiconductor testing device according to] The apparatus of claim 1 [3] further comprising [,] a display configured to display the changing rate falling outside of the range of pass/fail decision criteria.

[wherein

the measurement range determination circuit compares the plural current-value change rates obtained from the plural faulty samples with the range of pass/fail decision criteria per address pair, and selects an effective address pair group, to be effectively more used for the pass/fail decision and according to the number of the plural faulty samples, from the address pair group of the plural test vectors in the address pairs corresponding to the current-value change rates of the plural faulty samples which are outside of the range of pass/fail decision criteria.]

5. (Amended) A semiconductor testing method for testing semiconductor devices, comprising [the steps of]:

reading measurement data including a test vector data and data of good samples and faulty samples returned to a manufacturer;

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[inputting a plurality of] supplying the test vectors to [semiconductor devices each being good devices as a non-defective device,] the good samples and the faulty samples;

[and measuring a current value output from each good sample corresponding to an address of each test vector, and outputting the measured current values as the current values of the good samples;

calculating a current-value change rate per address pair forming two different addresses, and outputting this current-value change rate as the current-value change rate of the good sample;]

determining a range of pass/fail decision criteria and effective address pairs for testing semiconductor devices; and [to be used for deciding whether a target test device to be tested is a good sample (non-defective sample) or a faulty sample per address pair based on the above current-value change rates; and

supplying the plural test vectors to semiconductor devices as faulty samples, and measuring current values output from the above semiconductor devices as the faulty samples corresponding to the addresses, and outputting the measured current values as the current values of the faulty samples; and

comparing the current-value change rates of the measured current values corresponding to each address pair per address pair, and deciding whether a semiconductor device as a target test device to be tested is a good (non-defective)

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device or a faulty (defective) device based on the current-value change rates of the address pairs extracted based on the above comparison result.]

applying test vectors of the effective address pairs to the semiconductor devices for testing.

6. (Amended) [A semiconductor testing method according to] The method of claim 5, [wherein] further comprising:

[the number of the semiconductor devices as the good samples is a plural number, and the current value and the current-value change rate of the good samples are output for each good sample, and the range of pass/fail decision criteria is determined based on the current-value change rates of the plural good samples.]

selecting address pairs from the test vector data;

supplying the address pairs to the good samples and the faulty samples;

measuring current-values of the good samples and the faulty samples;

calculating changing rates of each of the good samples and the faulty samples;

determining a range of pass/fail decision criteria by using the changing rates of each of the good samples;

comparing the changing rates of each of the faulty samples to the range of pass/fail decision criteria;

determining whether the changing rates of each of the faulty samples fall outside of the range of pass/fail decision criteria;

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determining the changing rate falling outside of the range of pass/fail decision criteria; and

selecting an address pair which makes the faulty samples provide the changing rate falling outside of the range of pass/fail decision criteria as an effective address pair.

7. (Amended) [A semiconductor testing method according to] The method of claim 5, further [comprises the steps of] comprising:

acquiring the effective address pair;

supplying [the plurality of] test vectors corresponding to the effective address pair to the semiconductor devices [as faulty samples, and measuring current values output from these semiconductor devices corresponding to the address pairs, and outputting the current values of the faulty samples];

measuring current-value output of the semiconductor devices;

calculating [a] change rates of the semiconductor devices [between the two current values in the above current values corresponding to each address pair, and outputting the calculated results as current-value change rates of the faulty samples]; and

determining a changing rate falling outside of the range of pass/fail decision criteria.

[comparing the current-value change rates of the faulty samples with the range of pass/fail decision criteria per address pair, and extracting effective address pairs, to be

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effectively used for the pass/fail decision, from the plural address pairs corresponding to the current-value change rates that are outside of the range of pass/fail decision criteria,

wherein the step of measuring current values of the target test device is the step of measuring the current values by supplying the test vectors corresponding to the extracted effective address pairs for the pass/fail decision to the semiconductor device as the target test device.]

8. (Amended) [A semiconductor testing method according to] The method of claim 7, [wherein] further comprising displaying the changing rate falling outside of the range of pass/fail decision criteria on a display.

[the number of the semiconductor devices as the faulty samples are a plural number, and the current values and the current-value change rates of the faulty samples are output per faulty sample, the semiconductor testing method further comprises the steps of comparing the current-value change rates obtained from the plural faulty samples with the range of pass/fail decision criteria per address pair; and

extracting the address pair group as an effective combination to be effectively used for the pass/fail decision from the plural address pairs corresponding to the current-value change rates of the faulty samples that are outside of the pass/fail decision criteria, according to the number of the faulty samples, and wherein

the step of measuring the current values of the target test device is the step of supplying the test vectors corresponding to the effective address pairs to be effectively used for the pass/fail decision to the semiconductor device as the target test device.]

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9. (Amended) A program with which a semiconductor testing method for testing semiconductor devices is executed by a computer in a semiconductor testing apparatus which comprises[:] a read circuit [for reading measurement data including test vectors; a measurement circuit for supplying the test vectors to a semiconductor device and for measuring current values output from the semiconductor device; and a decision circuit for deciding whether a semiconductor device as a target test device is a good device (non-defective device) or it is a defective device based on the current values], a determination circuit, an IDDQ measuring circuit, the program comprising:

[the program comprising the procedures of:]

instructions configured to read measurement data including a test vector data and data of good samples and faulty samples returned to a manufacturer;

instructions configured to [inputting a plurality of] supply the test vector[s] data to [semiconductor devices as] good [(non-defective)] samples[,] and faulty samples;

[measuring a current value corresponding to an address of each test vector output from the good sample, and outputting the measured current values as the current values of the good samples;]

[calculating a current-value change rate between two current values corresponding to an address pair forming two different addresses, and outputting the calculated current-value change rates as the current-value change rates of the good samples;]

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instructions configured to [determining] determine a range of pass/fail decision criteria [to be used for the criteria of the pass/fail decision whether a target test device to be tested is a good sample or a faulty sample per address pair based on the current-value change rates of the good samples] and effective address pairs for testing semiconductor devices; and

instructions configured to apply [supplying the plurality of the] test vectors of the effective address pairs for testing. [to semiconductor device as faulty samples, and measuring current values output from the semiconductor devices as the faulty samples corresponding to the addresses, and outputting the measured current values as the current values of the faulty samples;

calculating a current-value change rate of the two current values corresponding to each address pair, and outputting current-value change rates as the current-value change rates of the faulty samples; and

comparing the current-value change rate of the faulty samples with the range of pass/fail decision criteria per address pair, and deciding whether the semiconductor devices as the target test device is a good sample or a faulty sample based on the above comparison results.]

10. (Amended) [A] The program [with which a semiconductor testing method is executed by a computer in a semiconductor testing apparatus according to] of claim 9, [wherein] further comprising:

instructions configured to select address pairs from the test vector data;

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instructions configured to supply the address pairs to the good samples and the faulty samples

instructions configured to measure current-values of the good samples and the faulty samples;

instructions configured to calculate changing rates of each of the good samples and the faulty samples;

instructions configured to determine a range of pass/fail decision criteria by using the changing rates of each of the good samples;

instructions configured to compare the changing rates of each of the faulty samples to the range of pass/fail decision criteria;

instructions configured to determine whether the changing rates of each samples fall outside of the range of pass/fail decision criteria;

instructions configured to determine the changing rate falling outside of the range of pass fail/decision criteria; and

instructions configured to select an address pair that makes the faulty samples to provide the changing rate falling outside of the range of pass/fail decision criteria as an effective address pair.

[the number of the semiconductor devices as the good samples is a plural number,

the current values and the current-value change rates of the good samples are output per good sample, and

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the range of pass/fail decision criteria is determined based on the current-value change rates of the good samples.]

11. (Amended) [A] The program [with which a semiconductor testing method is executed by a computer in a semiconductor testing apparatus according to] of claim 9, further [comprises the procedures of] comprising:

instructions configured to acquire the effective address pair;

instructions configured to supply [supplying the plurality of the] test vectors corresponding to the effective address pair to the semiconductor devices [as faulty samples, and measuring current values output from the above semiconductor devices corresponding to the addresses of the test vectors, and outputting the measured current values as the current values of the faulty samples]; [and]

instructions configured to measure current-value output of the semiconductor devices;

instructions configured to [calculating] calculate changing rates of the semiconductor devices [a current-value change rate of the two current values corresponding to each address pair, and outputting the calculated results as the current-value change rates of the faulty samples]; and

instructions configured to determine a changing rate falling outside of the range of pass/fail decision criteria.

[comparing the current-value change rates of the faulty samples with the range of pass/fail decision criteria per address pair, and extracting effective address pairs, to be

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effectively used for the pass/fail decision, from the plural address pairs corresponding to the current-value change rates that are outside of the range of pass/fail decision criteria,

wherein the step of measuring the current values of the target test device is the step of supplying the test vectors corresponding to the above extracted effective test vectors to the semiconductor device as the target test device.]

12. (Amended) The [A] program [with which a semiconductor testing method is executed by a computer in a semiconductor testing apparatus according to] of claim 11, [wherein] further comprising instructions configured to display the changing rate falling outside of the range of pass/fail decision criteria on a display.

[the number of the semiconductor devices as the faulty samples is a plural number, and the current values and the current-value change rates of the faulty samples are output per faulty sample;

the above program for executing the semiconductor testing method further comprises the following procedures:

the procedure of comparing the current-value change rates obtained from the plural faulty samples with the range of pass/fail decision criteria per address pair; and

the procedure of extracting the address pairs to be effectively used for the pass/fail decision from the plural address pairs corresponding to the current-value change rates of the faulty samples that are outside of the pass/fail decision criteria, according to the number of the faulty samples,

and wherein

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the procedure of measuring the current values of the target test device is the procedure of supplying the test vectors corresponding to the extracted effective address pairs to the semiconductor device as the target test device.]

13. (Amended) A semiconductor testing method of specifying a faulty part in a semiconductor device, comprising [the steps of]:

reading measurement data wherein the measurement data includes a test program, test vector data, data of good samples and faulty samples returned to a manufacturer;

supplying [a plurality of] test vector[s] data to good and faulty samples [as semiconductor devices, and measuring current values corresponding to addresses indicating the test vectors];

determining a range of pass/fail decision criteria and effective address pairs for testing semiconductor devices in a manufacturing process;

applying test vectors of the effective address pairs to a semiconductor device; and

specifying a faulty part within the semiconductor device by measuring an emission from the semiconductor device.

[calculating current-value change rates between current values corresponding to an address pair consisting of two addresses in each of the good and faulty samples; and

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comparing the current-value change rates corresponding to the address pairs in each of the good and faulty samples, and determining address pairs of the test vectors to be used for performing an emission analysis that is useful to specify a faulty part in a semiconductor device.]

14. (Amended) [A semiconductor testing] The method of [specifying a faulty part in a semiconductor product according to] claim 13, further [comprises] comprising [the steps of]:

selecting address pairs from the test vector data;

supplying the address pairs to the good samples and the faulty samples;

measuring current-values of the good samples and faulty samples;

calculating changing rates of each of the good samples and faulty samples;

determining a range of pass/fail decision criteria by using the changing rates of each of the good samples;

comparing the changing rates of each of the faulty samples to the range of pass/fail decision criteria;

determining whether the changing rates of each of the faulty samples fall outside of the range of pass/fail decision criteria;

determining the changing rate falling outside of the range of pass/fail decision criteria; and

selecting an address pair which makes the faulty samples provide the changing rate falling outside of the range of pass/fail decision criteria as an effective address pair.

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[performing an emission analysis for each of the good and faulty samples by using the test vectors obtained in the steps of determining the address pairs of the test vectors to be used for performing the emission analysis; and

specifying a faulty part by comparing emission patterns from the good sample with emission patterns from the faulty sample that have been obtained in the above emission analysis step.]

15. (Amended) [A semiconductor testing] The method of [specifying a faulty part in a semiconductor product according to] claim 14, wherein the faulty part specifying step further comprises:

acquiring the effective address pair;

supplying test vectors corresponding to the effective address pair to the semiconductor device;

measuring current-value output of the semiconductor device;

calculating changing rates of the semiconductor device;

measuring an emission from the semiconductor device; and

determining a changing rate falling outside of the range of pass/fail decision criteria.

[in the emission analysis step, different test vectors are supplied to each of the good and faulty samples in order to obtain emission patterns by changing the current values output from these samples, and

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in the faulty part specifying step, the faulty part is specified by obtaining a difference of the change of the emission patterns in each of the good and faulty samples.]

16. (Amended) A semiconductor testing [method of] apparatus for specifying a faulty part in a semiconductor device, comprising: [product according to claim 15, further comprises the step of comparing the change of the emission parts in the good and faulty samples,

wherein in the faulty part specifying step, the emission area and the change of the emission area that do not occur in the good sample are detected and thereby the emission that is unique to the faulty sample is decided as the faulty part relating to the defect.]

a read circuit configured to read measurement data wherein the measurement data includes a test program, test vector data, data of good samples and faulty samples returned to a manufacturer;

a determination circuit configured to supply the test vector data to the good samples and faulty samples, and to determine a range of pass/fail decision criteria and effective address pairs for testing semiconductor devices in a manufacturing process; and

a faulty part specifying circuit configured to apply test vectors of the effective address pairs to a semiconductor device and to specify a faulty part by measuring an emission from the semiconductor device.

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17. (Amended) The [A semiconductor testing] method of [specifying a faulty part in a semiconductor product according to] claim 13, wherein determining a range of pass/fail decision criteria is achieved by:

[in the step of calculating the current-value change rate, two test vectors designated by two addresses are combined as an address pair, the range of the current-value change rates in the good and faulty samples are obtained according to the current-value change rates calculated by comparing the current values in optional number of the address pairs or in the test vectors in all the address pairs in each of the good and faulty samples.]

a changing rate calculation circuit configured to select address pairs from the test vector data, to supply the address pairs to the good samples and the faulty samples, to measure current-values of the good samples and faulty samples, and to calculate changing rates of each of the good samples and faulty samples;

a range criteria determination circuit configured to determine a range of pass/fail decision criteria by using the changing rates of each of the good samples;

a comparing circuit configured to compare the changing rates of each of the faulty samples to the range of pass/fail decision criteria, and to determine whether the changing rates of each of the faulty samples fall outside of the range of pass/fail decision criteria; and

an effective address pair determination circuit configured to determine the changing rate falling outside of the range of pass/fail decision criteria, and to select an

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address pair that makes the faulty samples to provide the changing rate falling outside of the range of pass/fail decision criteria as an effective address pair.

18. (Amended) The [A semiconductor testing] method of [specifying a faulty part in a semiconductor product according to] claim 17, wherein the faulty part specifying circuit further comprises:

[the current-value change rate between the test vectors per address pair in the faulty sample is compared with the current-value change rate between the test vectors in each address pair in the good sample, and]

a tester configured to acquire the effective address pair, to supply test vectors corresponding to the effective address pair to the semiconductor device, to measure current-value output of the semiconductor device, and to calculate changing rates of the semiconductor device;

an emission measuring circuit configured to measure an emission from the semiconductor device; and

a decision circuit configured to determine a [the test vector pairs in the condition that the current-value] [change] changing rate falling [obtained from the faulty sample is] outside of the range of pass/fail decision criteria.[the current-value change rate obtained from the faulty sample are searched, and these test vector pairs are decided as the test group to be used for the emission measurement, and the test vector group is extracted as the address pairs of the test vectors to be used for specifying a faulty part in a semiconductor device.]

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19. (Amended) A program with which a semiconductor testing method is executed by a computer in a semiconductor testing apparatus [for specifying a faulty part in a semiconductor device,] which comprises a read circuit, a determination circuit, and a faulty part specifying circuit, the program comprising:

instructions configured to read measurement data wherein the measurement data includes a test program, test vector data, data of good samples and faulty samples returned to a manufacturer;

instructions configured to supply the test vector data to good samples and faulty samples;

instructions configured to determine a range of pass/fail decision criteria and effective address pairs for testing semiconductor devices in a manufacturing process;

instructions to apply test vectors of the effective address pairs to a semiconductor device; and

instructions to specify a faulty part within the semiconductor device by measuring an emission from the semiconductor device.

[a current-value change measuring circuit for supplying a plurality of test vectors to good and faulty samples as semiconductor devices, and for measuring a current value corresponding to each test vector;

a current-value change rate calculation circuit for calculating a current-value change rate per test vector pair in each of the good and faulty samples, the number of

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the test vector pairs being a desired number, by using the current values from the current-value measuring circuit;

an emission measurement address pair determination circuit for comparing the current-value change rates in each test vector pair in each of the good and faulty samples obtained by the current-value change rate calculation circuit, and for determining test vectors to be used in an emission analysis based on the comparison results;

an emission analysis circuit for performing the emission analysis using the test vectors determined above in each of the good and faulty samples; and

a faulty part determination circuit for comparing emission patterns of the good and faulty samples, and for specifying a faulty part in a semiconductor device based on the result of the emission pattern comparison.]

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